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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448

7590 03/28/2003

ON Semiconductor
Patent Administration Dept - MD A700
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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,145	AVERETT ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *January 14, 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, and 26 - 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawing Corrections

1. The drawing corrections submitted in Letter No. 8 of January 14, 2003 are approved.

Claim Rejections – 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5, 6, and 8 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. '041 (US 5,640,041).

5. Regarding Claim 1, Lur et al. disclose a semiconductor device formed in a monocrystalline silicon substrate (Col. 3, line 67) where a second recessed region (22) (See Figure 6) is formed within a first recessed region (15,16) etched from a deposited silicon dioxide layer (Col. 4, lines 53 - 55) and the surface of trenches covered with silicon dioxide (CVD) (cap layer) to seal the "voids" or trenches (Col. 3, lines 10 – 15). The walls of trenches are covered with silicon dioxide (25) (See Figure 10).
Lur et al. '041 do not disclose that the second dielectric material (SiO2) is thermally grown. However, for this application, a thermally grown and CVD silicon dioxide layer are functionally equivalent in terms of a sealant atop trenches.

6. Regarding Claim 2, Lur et al. disclose that an active device is formed in an active region (See Figure 14) with a gate dielectric (4), gate electrode (5), and doped regions (52,54) (n+,n-) at the peripheral edges.

7. Regarding Claim 5, Lur et al. disclose (Col. 3, line 67) that the substrate is silicon.

8. Regarding Claim 6, Lur et al. disclose (Col. 4, lines 1 – 4) that the dielectric material is silicon dioxide.

9. Regarding Claim 8, as discussed previously, Lur et al. do not disclose that the second silicon dioxide layer is thermally grown, but rather formed by CVD. For this application, the layers are functionally equivalent.

10. Regarding Claim 9, as discussed previously, Lur et al. disclose that the dielectric layer forms a cap layer.

11. Regarding Claim 10, Lur et al. disclose that the first dielectric layer is formed by CVD (Col. 4, lines 1 – 4).

12. Regarding Claim 11, Lur et al disclose that the depth of trenches in the second recessed region for the narrow trenches (17) (See Figure 6) is 20,000 Angstroms (2um) (Col. 4,lines 39 – 40),which is consistent with the depth recited in the instant application, subject to optimization for a particular device application.

13. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as unpatentable over Lur et al.

as applied to Claims 1, 2, 5, 6, and 8 – 11 above, and further in view of Zekeriya et al. (US 2003/0030107 A1).

Lur et al. do not disclose the presence of a passive device or component formed over the second recessed region. However, Zekeriva et al. disclose the formation of a resistor (106) Figure 13) on a dielectric layer (104) with a metal plug (126") for electrical contact. Hence it would have been obvious at the time of the invention to one of ordinary skill in the art to use the technique of Zekeria et al. to form a resistor on the overlying dielectric layer in Lur et al. to obtain a component with reduced parasitic capacitance owing to the large volume of air pockets and low permittivity of the underlying region.

14. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al., as applied to Claims 1, 2, 5, 6, and 8 – 11 above, and further in view of Holbrook et al. (US 6,495,853 B1).

Lur et al. do not disclose the presence of a third dielectric material deposited on the walls of trenches. However, it is routine to form a liner layer on the walls and Holbrook et al. disclose (422) (Figure 6) the formation of a silicon nitride layer (Col. 6, lines 63 – 67) on the walls of the trench. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Holbrook et al. with Lur et al. to provide a liner layer that would reduce sharp edges and roughness of subsequent deposited layers (Col. 6, lines 63 – 67).

15. Claims 26 – 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. in view of Wolf ("Silicon Processing for the VLSI Era: Volume 2 – Process Inte-

gration," Lattice Press, Sunset Beach, CA, (1990), pp.196 – 197).

16. Regarding Claim 26, Lur et al. disclose a semiconductor device formed in a monocrystalline silicon substrate (Col. 3, line 67) where a second recessed region (22) (See Figure 6) is formed within a first recessed region (15,16) etched from a deposited dielectric material (12, Figure 5) with a semiconductor layer (14) overlying the dielectric layer. Further Lur et al. disclose that the surface of trenches is covered with silicon dioxide (CVD) (cap layer) to seal the created "voids" or trenches (Col. 3, lines 10 – 15) formed by a deposition shadowing effect (Wolf, p.197, Figure 4-8). The walls of trenches are covered with silicon dioxide (25) (See Figure 10) and the structure totally sealed. Lur et al. do not disclose that the second dielectric material (SiO2) is thermally grown. However, for this application, a thermally grown and CVD silicon dioxide layer are functionally equivalent in terms of a sealant atop trenches.

17. Regarding Claim 27, Lur et al. disclose (14) (Figure 5) that the semiconductor layer is deposited polysilicon.

18. Regarding Claim 28, Lur et al. do not disclose that the second dielectric material is thermally grown silicon dioxide, but rather by CVD. As mentioned previously, for this application, a thermally grown and a CVD layer are functionally equivalent.

19. Regarding Claim 29, Lur et al. disclose that an active device is formed in an active region (See Figure 14) with a gate dielectric (4), gate electrode (5), and doped regions (52,54) (n+,n-) at the peripheral edges.

20. Claims 30 and 31 are rejected under 35 103(a) as being unpatentable over Lur et al., in view of Wolf, as applied to Claims 26 – 29, and further in view of Zekeriya et al.

Lur et al. do not disclose the presence of a passive device or component formed over the second recessed region. However, Zekeriva et al. disclose the formation of a resistor (106) Figure 13) on a dielectric layer (104) with a metal plug (126") for electrical contact. Hence it would have been obvious at the time of the invention to one of ordinary skill in the art to use the technique of Zekeria et al. to form a resistor on the overlying dielectric layer in Lur et al. to obtain a component with reduced parasitic capacitance owing to the large volume of air pockets and low permittivity of the underlying region.

21. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al., as applied to Claims 26 – 29 above, and further in view of Holbrook et al.

Lur et al. do not disclose the presence of a third dielectric material deposited on the walls of trenches. However, it is routine to form a liner layer on the walls and Holbrook et al. disclose (422) (Figure 6) the formation of a silicon nitride layer (Col. 6, lines 63 – 67) on the walls of the trench. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Holbrook et al. with Lur et al. to provide a liner layer that would reduce sharp edges and roughness of subsequent deposited layers (Col. 6, lines 63 – 67).

Response to Arguments

22. Applicant's arguments have been carefully considered but they have not been found to be persuasive. In addition these are considered moot in terms of the new grounds for rejection. However, a few points should be made in regard to commentary. The reference cited by Applicant is not germane to this application. Further, Applicant appears to have misread the Lur et al. reference, or does not fully comprehend what is being related. The formation of voids and subsequent sealing is well known in the art (See Wolf reference) and such incomplete step coverage is defined by the conformality factor (See Applied Materials Student Training Manual, pp. 3-15 and 3-16) (attached). Creation of voids is not automatic in CVD and is a function of procedure used and deposition condition. Therefore, with current technology, these are "created," since void nucleation has been eliminated. With deposition, the voids are totally sealed (page 3-16) as is disclosed by Lur et al. (See also Figure 14, Applied Materials Student Guide, and Wolf).

Conclusions

23. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772.**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722.**

Thomas Magee
March 19, 2003

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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